II. THE JENG REFERENCE

Jeng U.S. Patent 5,821,621 discloses an improved method for integrating polymer and other low dielectric constant materials, which may have undesirable physical properties into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines. Jeng combines the advantages of SiO_2 dielectric material with low dielectric constant materials by placing the low dielectric material only between tightly spaced apart lines. The inventor discusses the various types of undesirable capacitance which occur in integrated circuit structures, such as line to line capacitance and line to ground capacitance, and concludes that of those two types of capacitance, more than 90% is line to line capacitance. Jeng states that many polymeric materials have low dielectric constants, but also have a number of shortcomings with respect to at least their physical properties.

Jeng proposes to take advantage of the desirable low k characteristics of such polymeric dielectric materials by first spinning a low-k dielectric material across the surface of the wafer to fill the critical areas, i.e., the areas between closely spaced together interconnect lines. This also serves to fill all of the areas between all interconnect lines, i.e., the non-critical areas as well. The areas where the low-k material is to remain, are masked off with a resist mask. The unmasked low dielectric constant material in non-critical or widely spaced areas is then etched away, leaving the problematic but desirable low-k material in only those areas where needed, e.g., between closely spaced apart interconnect lines.

After removal of the resist mask, a layer of conventional dielectric material such as SiO_2 is applied over the entire structure, including the etched away areas, to fill the remaining area with SiO_2, e.g., to provide spacing between more widely spaced apart metal lines.

III. THE INVENTION

The invention comprises a composite low k dielectric layer comprising a first layer of low k silicon dioxide dielectric material formed on an oxide layer of an integrated circuit structure on a semiconductor substrate having closely spaced apart metal lines thereon. A second layer of low k silicon oxide dielectric material, having a faster deposition rate than the

first layer, is then deposited over the first layer up to the desired overall thickness of the low k silicon oxide dielectric layer. In a preferred embodiment, the steps to form the resulting composite layer of low k silicon oxide dielectric material are all carried out in a single vacuum processing apparatus without removal of the substrate from the vacuum apparatus.

The composite layer of low k silicon oxide dielectric material is formed by depositing, in high aspect ratio regions between closely spaced apart metal lines, a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties until the resulting deposition of low k silicon oxide dielectric material reaches the level of the top of the metal lines on the oxide layer.

The resultant composite layer of low k silicon oxide dielectric materials exhibits void-free deposition properties in high aspect ratio regions between the closely spaced apart metal lines, deposition rates in other regions comparable to standard k silicon oxide, and reduced via poisoning characteristics.

IV. DISCUSSION

Claims 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng U.S. Patent 5,821,621. The Office Action states that in re claims 15-16, and 18-19, Jeng discloses in figs 1-4 a composite layer of low k silicon-oxide dielectric material (22) on an oxide layer (12) of an IC (fig 1), said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties (col. 4, lines 1-5), comprising a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties (22), and a second layer of low k silicon oxide dielectric material (24), to a desired thickness.

Applicants respectfully disagree with the above interpretation of Jeng's figs. 1-4 and col. 4, lines 1-5 of the Jeng patent, at least with its representation that the cited text and drawings constitute teachings by Jeng that his liner layer 22 is also a low k dielectric layer. (Applicants concede that material 24 is identified as a low k dielectric material 24 in the text). Column 4, lines 1-5 of the Jeng patent reads as follows:

> "The method of the present invention contemplates using high aspect ratio metal where the thickness of the interconnect metal is greater than the width. The high aspect ratio interconnects are useful to reduce line resistance while maintaining close spacing for high density circuits."

While the above quoted text cited against Applicants' claims would appear to offer a reason why low k dielectric material 24 is used between closely spaced apart lines, as shown in Figures 1 and 4-6, Applicants fail to see how the cited passage establishes that liner 22 also is a low k dielectric material. Jeng, at column 4, lines 16-33, provides his definitions of both dielectric material 24 and liner layer 22 as follows:

> "FIG. 3 shows the application of a liner layer 22 over the metal interconnects and exposed surfaces of the dielectric layer. Liner layer 22 is an optional layer to protect metal interconnect lines 14 from solvents used in some spin-on low-k materials to prevent oxidation of the metal interconnect lines. Liner layer 22 can be eliminated when non-interactive dielectric materials are used, that is dielectric materials that will react with the metal layer or materials used for the via contact. **Liner layer 22 is typically** a thin layer, 250 Å-1,000 Å coverage on blank wafer, of **plasma enhanced TEOS** with about 40% step coverage."
>
> "After application of a liner layer, if used, a low dielectric constant material 24 is applied on the surface of the wafer. The low-k material 24 is applied in sufficient thickness to fill critical areas 18 between the metal interconnects 14, shown in FIG. 4." (emphasis added)

Thus, Jeng clearly indicates here that 24 is a low k dielectric material, while no such representation is made concerning liner layer 22. The rejection of Applicants' claims depends (at least) on the presence of two low k dielectric layers, and the cited drawings (figs 1-4) and passage (col. 4, lines 1-5) in Jeng do not teach that line[redacted]2 is a low k dielectric layer. Claim 15-16 and 18-19 should, therefore, be patentable over Jeng.

Regarding the specific comments made relating to the rejection of claim 17, the cited passage at col. 1, lines 45-55, contains no teachings or suggestions that the claimed composite layer of low k dielectric material should include a first layer of low k carbon-doped silicon oxide dielectric material and also a second layer of low k carbon doped silicon oxide dielectric material. In particular, as discussed above, the cited passages do not identify layer 22 as a low k dielectric layer.

With respect to the mention (in the Office Action) of the table in column 5 of Jeng, Applicants are puzzled as to how the items listed in this table supports the position taken by the USPTO in the rejection of claim 17. Elsewhere in the Rejection, numerals 22 and 24 have been referred to (by the USPTO) as constituting low k dielectric layers, and in the patent reference, Jeng has referred to 22 as a layer liner and 24 as a low k dielectric material.

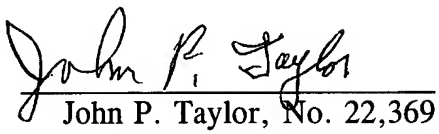
However, there seems to be no correlation between such allegations and the materials found in the column 5 Figure. For example, numeral 22 is referred to in the table as specifically constituting a "photoresist", and generically a "mask" in the table; while numeral 24 is specifically identified as "SiO_2" and generically as an "inter-metal dielectric". Claim 17 should, therefore, be patentable over Jeng.

V. **SUMMARY**

Applicants' claims require a first low k dielectric layer comprising low k dielectric material capable of forming void-free depositions in high aspect ratio regions, and a second layer of low k dielectric material formed over the first layer of low k dielectric material. Applicants' claimed structure is not anticipated or suggested by the Jeng patent. Applicants' claims should be in condition for allowance.

If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,



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DOCKET NO. 99-102/1D

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The first paragraph inserted after the title and subtitle by the Preliminary Amendment filed with the patent application on March 15, 2002, has been amended as follows:

This application is a division of U.S. Patent 6,391,795 B1, issued May 21, 2002 ~~Serial No. 09/426,056, filed October 22, 1999~~.

The third of the three paragraphs inserted after the title and subtitle by the Preliminary Amendment filed with the patent application on March 15, 2002, has been amended as follows:

The subject matter of this application relates to the subject matter of ~~copending~~ Li, Catabay, and Hsia U.S. Patent ~~Application Serial~~ No.6,423,628, issued July 23, 2002, ~~09/425,552~~ entitled "INTEGRATED CIRCUIT STRUCTURE HAVING LOW DIELECTRIC CONSTANT MATERIAL AND HAVING SILICON OXYNITRIDE CAPS OVER CLOSELY SPACED APART METAL LINES", filed by one of us with others on October 22, 1999, assigned to the assignee of this application, and the subject matter of which is hereby incorporated herein by reference.

The paragraph beginning at line 27 of page 3, has been amended as follows:

In the aforementioned U.S. Patent ~~Serial~~ No. 6,423,628, issued July 23, 2002, ~~09/425,552,~~ a layer of silicon oxynitride (SiON) is formed over the top surface of the metal lines to serve as an anti-reflective coating (ARC), a hard mask for the formation of the metal lines, and a buffer layer for chemical mechanical polishing (CMP). Low k silicon oxide dielectric material having a high carbon doping level is then formed in the high aspect regions between closely spaced apart metal lines up to the level of the silicon oxynitride. CMP is then applied to planarize the upper surface of the low k carbon-doped silicon oxide dielectric layer, using the SiON layer as an etch stop, i.e., to bring the level of the void-free low k silicon oxide dielectric layer even with the top of the SiON layer. A conventional (non-low k) layer of silicon oxide dielectric material is then deposited by plasma enhanced chemical vapor deposition (PECVD) over the low k layer and the SiON layer. A via is then cut through the second dielectric layer and the SiON to the top of the metal line. Since the via never contacts the low k layer between the metal lines, via poisoning due to exposure of the low k layer by the via does not occur.